

ABSTRACT OF THE DISCLOSURE

A memory module includes at least one CAR and a plurality of DRAMs provided so as to be close and adjacent to one another on one face and the other face of a module substrate. The DRAMs are divided into a plurality of memory groups. Memory groups adjacent to each other of these memory groups are paired with each other. One of this pair is a 1-ranked memory group and the other is a 2-ranked memory group. This pair of the memory groups is connected to the CAR via short wiring with a T-branch structure having a short stub. One of the pair of the memory groups on the signal-reception side functions as an open end. Active termination is performed by a termination resistor of the other of the pair of the memory groups on the signal-non-reception side. Subsequently, signal reflections can be reduced.